Nanocomposites and nanomaterials

Single- and double layered Si nanocrystal structures in SiO_2 for non-volatile memory devices

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Silicon nanocrystal (NC) memory devices are considered as potential heir of conventional floating gate memory devices, since the latter have come to their ultimate limits by the continuous downscaling. The different structure of the floating gate led to new physics of operation and hence to the changes of electrical parameters. The paper is devoted to detailed study of charge trapping processes occurred during memory window formation and retention in NC memory devices. As objects the silicon MOS capacitors with one and two NC layers inside of SiO_2 were used.

The memory window formation methods are based on the programming pulses application combined with high speed capacitance measurements. The differences in bipolar and unipolar programming modes were compared and analyzed. Both of them are suitable for successful window formation, but unipolar one is more suitable. The application of the different positive bias to the gate leads to electron injection from the substrate to the oxide layer associated with nanocrystals (Fig.1.). As the result the stored charge screens the gate field and effectively shifts the flatband voltage to more positive. It was deduced that for programming pulses of 4, 5 and 6V the charge trapped at each average nanocluster in oxide were 2,3 and 4 electrons respectively.

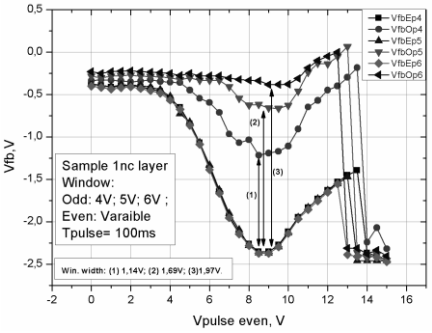

Fig.1. Window formation characteristics with different programming voltages used.

Influence of different gate potentials and elevated temperatures on the charge trapping and retention processes was evaluated. The increase of the electric biasing field of both polarities results in positive charge generation in the dioxide. The unipolar recharging significantly prolongs the window closure. The double NC layered samples have much more long window retention comparing with the single NC layered samples.