Nanoscale physics

Field effect transistor with high density heterojunction gate

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One of the main disadvantages of a FET with Me-S gate is a great variation of threshold voltage with low allowable logic level voltage difference. This drawback results into low noise stability and limits maximum slope of Schottky FET [1,2]. In order to increase the height of the gate barrier and reduce ΔU_T FET with complex gate structure is required.

By forming of a thin layer of triple alloy of amorphous silicon (α-Si-Ge-B) between metal gate and channel in silicon FET, which has a high barrier with crystalline monosilicon was managed to get a small variation of U_T (<11 mV) for FET with λ = 0,5 μm at 100 mm diameter substrate, steep slope (> 130 mS/mm) with 0.5 V logic amplitude. This technology allows creation of gates with λ = 0,5 μm, ensuring high performance of FET: τ_D = 114 ps at $P_D\tau_D$ = 1,6 pJ and τ_D = 26 ns at $P_D\tau_D$ = 3,3 pJ. Similarly FET n-GaAs was obtained, which provide a logical amplitude of 0.94 V at τ_D = 34 ps and P_D = 1,9 mW.

Experimentally produced FET with hole plane-doped heterojunction gate had g_m = 500 mS/mm at λ = 2 μm and a maximum drain current of 430 mA/mm with mobility in the channel 4000 cm^2/Vs. By reducing of channel length to 1 μm it is possible to increase all these characteristics by 2 times. Main advantages of FETs of this type is the ability to form a n-, and p-type cannel and a possibility to work in depletion and enrichment modes, that makes possible to form a complementary structure for high speed logic circuits.

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2. *Moskalyuk V. A., Timofeev D. I., Fedyaj A. V.* Sverhbystrodejstvuyushchie pribory ehlektroniki. - Kyiv: NTUU KPI, 2012.-480 P.