Method of reducing CMOS inverter switching energy

**1A.A. Druzhinin, 2I.T. Kogut, 2V.I. Holota,**

**1S.I. Nichkalo, 1Y.M. Khoverko, 2T.G. Benko**

*1Lviv Polytechnic National University, 12 S. Bandera Str., Lviv, Ukraine, 79013* 2Vasyl Stefanyk Precarpathian National University, 57 Shevchenko Str., Ivano- Frankivsk, Ukraine, 76018, taras.benko@pnu.edu.ua

**(a)**

**(b)**

**(c)**

**INTRODUCTION**

Due to the increase in the integration of digital ICs, the number of CMOS Logic family is increasing, as they are more productive and have low noise compared to other Logic families. However, with increasing integration, the switching energy of CMOS inverters decreases more slowly than their size decreases. Reducing the size of MOS transistors allows switching CMOS inverters at higher frequencies. As a result, the dissipated power of switching increases and the release of heat increases, which requires complex cooling systems. Therefore, in digital circuits, reducing the switching energy of CMOS inverter is an actual problem.

**CALCULATION OF DISSIPATION POWER FROM SHORT-CIRCUIT CURRENTS**

When switching the inverter Fig. 1a between the states of log. 1 and log.0 there is an area in which *Vout*=*Vin=VМ* and both CMOS transistors are in a state of saturation, Fig. 1b. The middle of this region *VM=VDD/2* is taken as the switching threshold if the conditions *βn*≈*βp*, *Vthn*=|*Vthp*|, *Wp/Wn*=*μn/μp* are met. The middle of the switching area corresponds the maximum value of the short current *IDDQ=Isc* from the power supply to the grounded substrate, Fig. 1c.

***Fig. 1.*** *Switching threshold of CMOS inverter*

To reduce the short current, and hence the dynamic energy, it is proposed to connect additional CMOS transistors with separate clock to the leakage current flow

path. A separate clock will switch additional transistors to linear mode during transitions between logic levels, thereby limiting peak currents. It is shown how the clocking of additional transistors by signals of various forms affects the values of short-circuit currents. For the basic circuit of the inverter (Fig. 1a) input and output signals, currents of the transistors M1, M2 and currents of the load capacity C1 for high-to-low output transition and low-high output transition are shown in Fig. 2. The basic circuit and all shown circuits were modeled in LTspice XVII. As can be seen from Fig. 2, peak-currents of the transistors M1, M2 and the charge/discharge currents of the load capacity *C1* are at the high-to-low output and low-to-high output transitions. When the values change on the fronts of the signal from 0 to *Vdd* and from *Vdd* to 0, the transistors *M1*, *M2* are in the conducting state for some periods of time, which causes currents to flow from the power source *V2* to the ground. As we can see in Fig. 2, the short-circuit current is determined by the expression *I*sc=max(Id(M1), Id(M2)) - I(C1) and corresponds to the current curve of the transistor with the minimum amplitude. On the high-to-low output it is curve Id(M2), and the low-to-high output it is curve Id(M1). The power *Psc* dissipated by the

𝑖=𝑁

short-circuit current Id(M2) was calculated for the current curve Id(M2) by the formula 𝑃 = 𝑓 ∑ 𝛥 𝐼 𝛥𝑉 𝛥𝑡 , where *f* – the frequency of switching, Δ*I* , Δ*V* –

𝑠𝑐

𝑖=0

𝑖 𝑖 𝑖

*i*

*i*

average instantaneous values of currents and voltages during the time interval Δ*ti*, *N* – number of calculation intervals Δ*ti* for time *τ* (the input rise or fall times of the

inverter). The results of calculations for the time intervals *ti* are shown in Table 2 and Table 3. To increase the accuracy of the calculation, the number of *ti* can be taken larger.

***Fig. 2.*** *The diagram of input and output signals and currents:*

*Idpeak(M1)=1.6/0.5 mA, Idpeak(M2)=0.6/2.2 mA,*

*Ipeak(C1)=1.3/-1.6 mA, Idinst(M1)=1.5/0.4 mA,*

***Table. 2.*** *Dissipated power from short-*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ti, ns** | **Δti, ns** | **Vi, V** | **Vavr, V** | **Ii, mA** | **Iavr, mA** | **Pi, μW** |
| 0,45 |  | 5 |  | 0 |  |  |
| 0,73 | 0,28 | 4,87 | 4,94 | 0,2 | 0,1 | 13,89 |
| 0,82 | 0,09 | 4,8 | 4,84 | 0,3 | 0,25 | 10,88 |
| 0,88 | 0,06 | 4,75 | 4,78 | 0,4 | 0,35 | 10,03 |
| 0,95 | 0,07 | 4,55 | 4,65 | 0,5 | 0,45 | 14,65 |
| 1,07 | 0,12 | 4,12 | 4,34 | 0,62 | 0,56 | 29,05 |
| 1,12 | 0,05 | 3,75 | 3,94 | 0,5 | 0,56 | 11,00 |
| 1,17 | 0,05 | 3,37 | 3,56 | 0,41 | 0,45 | 8,06 |
| 1,23 | 0,06 | 2,75 | 3,06 | 0,2 | 0,3 | 5,55 |
| 1,28 | 0,05 | 2 | 2,38 | 0,1 | 0,15 | 1,81 |
| 1,41 | 0,13 | 0,75 | 1,38 | 0 | 0,05 | 9,38 |
| High-to-low output: | 105,85 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **ti, ns** | **Δti, ns** | **Vi, V** | **Vavr, V** | **Ii, mA** | **Iavr, mA** | **Pi, μW** |
| 5,4 |  | 0 |  | 0 |  |  |
| 5,67 | 0,27 | 0,25 | 0,13 | 0,2 | 0,1 | 0,339 |
| 5,73 | 0,06 | 0,5 | 0,38 | 0,3 | 0,25 | 0,566 |
| 5,76 | 0,03 | 0,75 | 0,63 | 0,4 | 0,35 | 0,659 |
| 5,89 | 0,13 | 1,75 | 1,25 | 0,59 | 0,5 | 8,05 |
| 5,96 | 0,07 | 2,75 | 2,25 | 0,5 | 0,55 | 8,60 |
| 5,99 | 0,03 | 3,25 | 3 | 0,4 | 0,45 | 4,05 |
| 6,06 | 0,07 | 4,25 | 3,75 | 0,3 | 0,35 | 9,23 |
| 6,12 | 0,06 | 4,75 | 4,5 | 0,2 | 0,25 | 6,79 |
| 6,18 | 0,06 | 4,87 | 4,81 | 0,1 | 0,15 | 4,29 |
| 6,42 | 0,24 | 5 | 4,94 | 0 | 0,05 | 5,81 |
| Low-to-high output: | 48,38 |

***Table. 3.*** *Dissipated power from short-*

*Idinst(M2)=0.2/2.0 mA at Ipeak(C1)=1.3/-1.6 mA*

*circuit current Id(M2) at f=0.1×109 Нz*

*circuit current Id(M1) at f=0.1×109 Нz*

**CONCLUSIONS**

New approach for reducing the power and energy dissipation is discussed. To reduce the short current, and hence the dynamic energy, it is proposed to connect additional CMOS transistors with separate clock to the leakage current flow path. A separate clock will switch additional transistors to linear mode during transitions between logic levels, thereby limiting peak currents. It is shown how the clocking of additional transistors by signals with step at the level of 0.5·*V*dd affects the values of short-circuit currents. The proposed approach allowed to reduce the amount of short circuit current in CMOS inverters by more than 40 %.

