**METHOD OF REDUCING CMOS INVERTER SWITCHING ENERGY**

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***Abstract – An approach to reducing the dynamic energy of the inverter using additional transistors, which a separate clock switches to a linear state at peak short-circuit currents***

***Keyword – CMOS inverter, separate clock, short-circuit current, linear state***

I. INTRODUCTION

Due to the increase in the integration of digital ICs, the number of CMOS Logic family is increasing, as they are more productive and have low noise compared to other Logic families. However, with increasing integration, the switching energy of CMOS inverters decreases more slowly than their size decreases. Reducing the size of MOS transistors allows switching CMOS inverters at higher frequencies. As a result, the dissipated power of switching increases and the release of heat increases, which requires complex cooling systems. Therefore, in digital circuits, reducing the switching energy of CMOS inverterі is an actual problem. Different approaches and methods of reducing CMOS incerters consumption energy are observed in articles [1-6].

II. PREVIOUS WORK

One of the important aspects when designing CMOS inverters is to reduce power consumption. The total energy consumption of a conventional CMOS inverter has two components: static energy consumption and dynamic energy consumption.

The static energy consumption is caused by the subthreshold current *Isub* in steady state. The static power dissipation is expressed by Eq. (1):

*Pstatic= Vdd·Isub* (1)

where *Vdd* is the supply voltage.

Dynamic energy has two main components which are results of the next sources: charging/discharging capacitance's and short-circuit currents.

The energy consumption from power supply during low-to-high output transition can be derived by integrating the instantaneous power over the period:

 (2)

The half of this energy is dissipated in PMOS transistor and other half is stored on *CL*.:

 (3)

The high-to-low output transition dissipates the energy stored on the *СL* into the NMOS transistor. The value of power consumption from the power source will depend on the switching frequency *f* of the CMOS inverter

 (4)

Dynamic switching power dissipation is predominant in the overall energy dissipation in CMOS circuits [4].

Short–circuit power is the second source of total power dissipation. It depends on the threshold and supply voltages, the drive strength of the gate, the frequency of operation, the input slope, and the output load connected to the gate. The expression to short-circuit power dissipation *Psc* with the assumption of zero load capacitance at the output is the following [8]:

 (5)

where *β=W/L* is the strength of the transistors, *Vth* and *Vdd* are the threshold and supply voltages, respectively, τis the input slope, and *f* is the frequency of operation.

Short-circuit current not only increases power consumption, but also adds noise to the supply current. To reduce the amount of the CMOS inverter energy consumption various approach are used: smart delay generator circuits [7], buffer circuits [8], LECTOR approach [9, 10], GALEOR approach [11], sleepy stack approach [12], zigzag keeper [13]. Some of this approach my be used for reduction short-circuit current in the CMOS inverter.

This paper introduces a new approach to reducing the amount of short circuit current in CMOS inverters by more than 40 %.This approach uses CMOS inverter with pull-up and pull-down network and additional transistor between them. Clock signals are applied to these transistors to switch them to the linear mode of operation when a short-circuit current flows.

III. CALCULATION OF DISSIPATION POWER FROM SHORT-CIRCUIT CURRENTS

When switching the inverter Fig. 1a between the states of log. 1 and log.0 there is an area in which *Vout*=*Vin=VМ* and both CMOS transistors are in a state of saturation, Fig. 1b.

The middle of this region *VM=VDD/2* is taken as the switching threshold if the conditions *βn*≈*βp*, *Vthn*=|*Vthp*|, *Wp/Wn*=*μn/μp*  are met. The middle of the switching area corresponds the maximum value of the short current *IDDQ=Isc* from the power supply to the grounded substrate, Fig. 1c.

|  |  |  |
| --- | --- | --- |
| а | b | c |

Fig. 1. Switching threshold of CMOS inverter

To reduce the short current, and hence the dynamic energy, it is proposed to connect additional CMOS transistors with separate clock to the leakage current flow path. A separate clock will switch additional transistors to linear mode during transitions between logic levels, thereby limiting peak currents. It is shown how the clocking of additional transistors by signals of various forms affects the values of short-circuit currents.

For the basic circuit of the inverter (Fig. 1a) input and output signals, currents of the transistors M1, M2 and currents of the load capacity C1 for high-to-low output transition and low-high output transition are shown in Fig. 2. The basic circuit and all shown circuits were modeled in LTspice XVII.



Fig. 2. The diagram of input and output signals and currents:

Idpeak(M1)=1.6/0.5 mA, Idpeak(M2)=0.6/2.2 mA, Ipeak(C1)=1.3/-1.6 mA,

Idinst(M1)=1.5/0.4 mA, Idinst(M2)=0.2/2.0 mA at Ipeack(C1)=1.3/-1.6 mA,

As can be seen from Fig. 2, peak-currents of the transistors M1, M2 and the charge/discharge currents of the load capacity *C1* are at the high-to-low output and low-to-high output transitions. When the values change on the fronts of the signal from 0 to *Vdd* and from *Vdd* to 0, the transistors *M1*, *M2* are in the conducting state for some periods of time, which causes currents to flow from the power source *V2* to the ground. As can be seen from Fig. 2, the short-circuit current is determined by the expression *I*sc=max(Id(M1), Id(M2)) - I(C1) and corresponds to the current curve of the transistor with the minimum amplitude. On the high-to-low output it is curve Id(M2), and the low-to-high output it is curve Id(M1). For example, instantaneous values of short-circuit currents at the high-to-low output and low-to-high output transitions for the circuit in Fig. 2 is taken for the maximum values of the charge and discharge currents of the load capacity *C1* and is shown in Table 1.

Table 1. Instantaneous values of currents

|  |  |
| --- | --- |
| High-to-low output transition | Low-to-high output transition |
| Id(M1),mA | Id(M2),mA | I(C1), mA | Id(M1),mA | Id(M2),mA | I(C1), mA |
| 1.5 | 0.2 | 1.3 | 0.4 | 2.0 | -1.6 |
| Discharge C1,short-circuit current 0.2 mA | Charge C1,short circuit current 0.4 mA |

As can be seen from the Table 1 instantaneous short-circuit current at the high-low output transition is determined by the instantaneous current of transistor M2, and at the low-high output transition by the current of transistor M1.

The power *Psc* dissipated by the short-circuit current Id(M2) was calculated for the current curve Id(M2) by the formula

 (6)

where *f* – the frequency of switching,Δ*Ii*, Δ*Vi*  – average instantaneous values of currents and voltages during the time interval Δ*ti*, *N* – number of calculation intervals Δ*ti* for time *τ* (the input rise or fall times of the inverter).

The results of calculations for the time intervals *ti*are shown in the Table 2 and Table 3. To increase the accuracy of the calculation, the number of *ti*can be taken larger.

Table 2. Dissipated power from short-circuit current Id(M2) at *f*=0.1×109 Нz

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *ti*, ns | *Δti*, ns | *Vi*, V | *V*avr, V | *Ii*, mA | *I*avr, mA | *Pi*, μW |
| 0,45 |  | 5 |  | 0 |  |  |
| 0,73 | 0,28 | 4,87 | 4,94 | 0,2 | 0,1 | 13,89 |
| 0,82 | 0,09 | 4,8 | 4,84 | 0,3 | 0,25 | 10,88 |
| 0,88 | 0,06 | 4,75 | 4,78 | 0,4 | 0,35 | 10,03 |
| 0,95 | 0,07 | 4,55 | 4,65 | 0,5 | 0,45 | 14,65 |
| 1,07 | 0,12 | 4,12 | 4,34 | 0,62 | 0,56 | 29,05 |
| 1,12 | 0,05 | 3,75 | 3,94 | 0,5 | 0,56 | 11,00 |
| 1,17 | 0,05 | 3,37 | 3,56 | 0,41 | 0,45 | 8,06 |
| 1,23 | 0,06 | 2,75 | 3,06 | 0,2 | 0,3 | 5,55 |
| 1,28 | 0,05 | 2 | 2,38 | 0,1 | 0,15 | 1,81 |
| 1,41 | 0,13 | 0,75 | 1,38 | 0 | 0,05 | 9,38 |
| High-to-low output: | 105,85 |

Table 3. Dissipated power from short-circuit current Id(M1) at *f*=0.1×109 Нz

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *ti*, ns | *Δti*, ns | *Vi*, V | *V*avr, V | *Ii*, mA | *I*avr, mA | Pi, μW |
| 5,4 |  | 0 |  | 0 |  |  |
| 5,67 | 0,27 | 0,25 | 0,13 | 0,2 | 0,1 | 0,339 |
| 5,73 | 0,06 | 0,5 | 0,38 | 0,3 | 0,25 | 0,566 |
| 5,76 | 0,03 | 0,75 | 0,63 | 0,4 | 0,35 | 0,659 |
| 5,89 | 0,13 | 1,75 | 1,25 | 0,59 | 0,5 | 8,05 |
| 5,96 | 0,07 | 2,75 | 2,25 | 0,5 | 0,55 | 8,60 |
| 5,99 | 0,03 | 3,25 | 3 | 0,4 | 0,45 | 4,05 |
| 6,06 | 0,07 | 4,25 | 3,75 | 0,3 | 0,35 | 9,23 |
| 6,12 | 0,06 | 4,75 | 4,5 | 0,2 | 0,25 | 6,79 |
| 6,18 | 0,06 | 4,87 | 4,81 | 0,1 | 0,15 | 4,29 |
| 6,42 | 0,24 | 5 | 4,94 | 0 | 0,05 | 5,81 |
| Low-to-high output: | 48,38 |

Thus, as a result, the dissipated power from the short-circuit current Id(M2) and Id(M1) at the load capacitance C1=1 pF at *f*=0.1×109 Нz is 105,85+48,38=154,23 μW.

IV. AN APPROACH TO REDUCING SHORT CIRCUIT CURRENTS

To reduce the peak currents of the inverter, and therefore the short-circuit currents, it is proposed to connect two additional transistors M3, M4 in series between transistors M1, M2, Fig. 3. On the fronts of the clock signals of transistors M1, M2, transfer transistors M3, M4 to the linear mode of operation using signals of a given form from a separate clock. Thus, on the fronts of the clock signals of transistors M1, M2, it is possible to increase the resistance of transistors M3, M4 and limit the short-circuit currents from the power source to ground.



Fig. 3. The dual clock inverter

For the inverter in Fig. 3, the influence of the waveform of clock V2 on peak currents, short-circuit current, and dissipated short-circuit power was analyzed. A comparison of the peak currents of the transistors M1, M2, short-circuit current and dissipated short-circuit power of the basic and analyzed circuits makes it possible to clarify the effectiveness of the proposed approach.

The diagram of input and output signals for the clock signal V2 with a step at the level of 3 V is shown in Fig. 4. The values of peak currents of transistors M1, M2, short-circuit current and dissipated short-circuit power for the circuit in Fig. 4 are shown in the Table 3 and Table 4.



Fig. 4. The diagram of input and output signals and currents:

V1: PULSE(0 5 2.0e-9 1.0e-9 1.0e-9 4e-9 10e-9 2),

V2: PWL(0 0 1.7e-9 0 2.25e-9 2.5 2.8e-9 2.5 3.4e-9 5.5 6.65e-9 5.5 7.2e-9 2.5 7.75e-9 2.5 8.2e-9 0 9e-9 0)

Table 4. Dissipated power from short-circuit current Id(M2) at *f*=0.1×109 Нz

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *ti*, ns | *Δti*, ns | *Vi*, V | *V*avr, V | *Ii*, mA | *I*avr, mA | *Pi*, μW |
| 1,92 |  | 5 |  | 0 |  |  |
| 2,12 | 0,2 | 4,95 | 4,98 | 0,05 | 0,03 | 2,54 |
| 2,18 | 0,06 | 4,9 | 4,93 | 0,1 | 0,08 | 2,22 |
| 2,26 | 0,08 | 4,8 | 4,85 | 0,15 | 0,13 | 4,85 |
| 2,34 | 0,08 | 4,7 | 4,75 | 0,2 | 0,18 | 6,65 |
| 2,57 | 0,23 | 4,5 | 4,6 | 0,25 | 0,23 | 23,96 |
| 2,72 | 0,15 | 4,25 | 4,38 | 0,2 | 0,23 | 14,86 |
| 2,75 | 0,03 | 4,1 | 4,18 | 0,15 | 0,18 | 2,19 |
| 2,79 | 0,04 | 4 | 4,05 | 0,1 | 0,13 | 2,03 |
| 2,81 | 0,02 | 3,9 | 3,95 | 0,05 | 0,08 | 5,93 |
| 2,85 | 0,04 | 3,6 | 3,75 | 0 | 0,03 | 3,83 |
| High-to-low output: | 60,27 |

Table 5. Dissipated power from short-circuit current Id(M1) at *f*=0.1×109 Нz

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| *ti*, ns | *Δti*, ns | *Vi*, V | *V*avr, V | *Ii*, mA | *I*avr, mA | Pi, μW |
| 6,91 |  | 0 |  | 0 |  |  |
| 7,15 | 0,24 | 0,3 | 0,15 | 0,1 | 0,05 | 0,182 |
| 7,26 | 0,11 | 0,9 | 0,6 | 0,2 | 0,15 | 0,99 |
| 7,33 | 0,07 | 1,2 | 1,05 | 0,25 | 0,23 | 1,65 |
| 7,43 | 0,1 | 1,8 | 1,5 | 0,28 | 0,27 | 3,98 |
| 7,54 | 0,11 | 2,8 | 2,3 | 0,25 | 0,27 | 6,72 |
| 7,61 | 0,07 | 3,3 | 3,05 | 0,2 | 0,23 | 4,80 |
| 7,65 | 0,04 | 3,6 | 3,45 | 0,15 | 0,18 | 2,42 |
| 7,7 | 0,05 | 3,9 | 3,75 | 0,1 | 0,13 | 2,34 |
| 7,77 | 0,07 | 4,35 | 4,13 | 0,05 | 0,08 | 2,17 |
| 7,9 | 0,13 | 4,9 | 4,63 | 0 | 0,03 | 1,53 |
| Low-to-high output: | 26,79 |

Thus, as a result, the dissipated power from the short-circuit current Id(M2) and Id(M1) at the load capacitance C1=1 pF at *f*=0.1×109 Нz is 60,27+26,79=87,06 μW.

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**VI. CONCLUSIONS**

In this paper, new approach for reducing the power and energy dissipation is discussed. To reduce the short current, and hence the dynamic energy, it is proposed to connect additional CMOS transistors with separate clock to the leakage current flow path. A separate clock will switch additional transistors to linear mode during transitions between logic levels, thereby limiting peak currents. It is shown how the clocking of additional transistors by signals with step at the level of 0.5·*V*dd affects the values of short-circuit currents. The proposed approach allowed to reduce the amount of short circuit current in CMOS inverters by more than 40 %.

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