**Could the negative capacitance effect be used in FETs with a ferroelectric gate?**

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**Abstract**

Weconsider a silicon MOSFET, in which the gate insulator is formed from thin layers of a dielectric SiO2 and a weak ferroelectric HfO2. We study the possibility of implementing a stable negative capacitance of the insulator in such a system, which would open the principal possibility to reduce the subthreshold swing to the values below the threshold, 60 mV/decade at room temperature, and supply voltage to the values below the fundamental Boltzmann limit, 0.5 V, which would be an important step towards further miniaturization of MOSFETs. It is shown theoretically that it is possible to achieve a transient negative capacitance of a ferroelectric in the situation when the charge at the capacitor plates increases more slowly than the ferroelectric polarization. Its temporal stabilization in the system composed from the thin dielectric and ferroelectric layers requires stable positive free energy and capacity of the whole system. Therefore, the effect of the negative capacitance of a ferroelectric itself cannot be manifested "outside" the system mentioned above, including the transistor applications and it is unrealistic to hope that the negative capacitance effect will help reduce the subthreshold swing below the critical value, and thus contribute to further miniaturization of the MOSFET.

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